CLAIMS

We claim:

1. A method for processing a digital signal in multiple stages, the method comprising:

receiving a plurality of samples representing a digital signal, each sample represented electronically with a finite number of bits in a dynamic range;

processing the samples through a series of coupled processing stages, wherein after at least one intermediate processing stage, the dynamic range of at least one of the samples is decreased without losing a significant bit; and

passing the processed samples to an output interface.

2. The method of claim 1, wherein the dynamic range of at least one of the samples is decreased by:

selecting for the sample the smallest dynamic range in which the sample can be represented without losing a significant bit; and

tracking the dynamic range for the sample.

3. The method of claim 1, wherein the dynamic range of at least one of the samples is decreased by:

selecting for the sample a dynamic range that is the larger of:

(1) the smallest dynamic range in which the sample can be represented without losing a significant bit, and

(2) the largest dynamic range already selected for any other sample between processing stages; and

tracking any dynamic range decrease for each output sample.

4. The method of claim 3, wherein tracking any dynamic range change includes recording a change in dynamic range for each sample.

5. The method of claim 1, further comprising:

pre-processing the samples before processing the samples.

6. The method of claim 1, further comprising:

before each processing stage, normalizing the samples to be expressed in the same dynamic range.

7. The method of claim 1, wherein each of the samples are represented electronically with a different number of bits after a processing stage compared to before.

8. The method of claim 1, wherein the samples are represented in two's complement binary notation.

9. A method for increasing the precision of a digital signal processed in multiple consecutive stages, the method comprising:

reading a plurality of input samples, the input samples corresponding to an output from a previous stage;

calculating a plurality of output samples using the input samples; and

for at least one output sample, decreasing the dynamic range of the output sample if the output sample can be represented in a smaller dynamic range without losing a significant bit.

10. The method of claim 9, wherein decreasing the dynamic range comprises selecting the smallest dynamic range in which the output sample can be represented without losing a significant bit.

11. The method of claim 9, wherein decreasing the dynamic range comprises:

selecting for each output sample a dynamic range that is the larger of:

(1) the smallest dynamic range in which the output sample can be represented without losing a significant bit, and

(2) the largest dynamic range selected for any previously processed output sample.

12. The method of claim 9, further comprising:

before calculating the output samples, normalizing the input samples to be expressed in the same dynamic range.

13. The method of claim 9, further comprising:

storing the output samples in a memory for use in a next stage.

14. A method for increasing the precision of a digital signal processor, the method comprising:

receiving a plurality of input samples representing a digital signal, each sample represented electronically with a finite number of bits in a dynamic range;

calculating a plurality of output samples using the input samples;

decreasing the dynamic range of one or more of the output samples if an output sample can be represented in a smaller dynamic range without losing a significant bit; and

passing the processed digital communications signal to an output interface of the digital signal processor.

15. The method of claim 14, wherein decreasing the dynamic range of each output sample comprises:

selecting for an output sample the smallest dynamic range in which the output sample can be represented without losing a significant bit; and

tracking the dynamic range for each output sample.

16. The method of claim 14, wherein decreasing the dynamic range of each output sample comprises selecting for the output sample a dynamic range that is the larger of:

(1) the smallest dynamic range in which the output sample can be represented without losing a significant bit, and

(2) the largest dynamic range selected for any previously processed output sample.

17. The method of claim 14, wherein the output samples are represented in two's complement binary notation.

18. A device for processing a digital signal in multiple stages, the device comprising:

a calculation module adapted to compute a set of output samples using a set of input samples; and

a post-calculation module operatively coupled to the calculation module, the post-calculation module adapted to decrease the dynamic range of at least one of the output samples for at least one stage if the output sample can be represented in a smaller dynamic range without losing a significant bit.

19. The device of claim 18, wherein the calculation module is coupled to the post-calculation module for receiving therefrom the output samples of a particular stage to use as input samples of a next stage.

20. The device of claim 18, wherein the calculation module comprises a plurality of calculation modules, each calculation module adapted to compute a set of output samples using a set of input samples for one or more of the multiple stages.

21. The device of claim 18, wherein the post-calculation module is adapted to set the dynamic range of each of the output samples, for a particular stage, to be the larger of:

(1) the smallest dynamic range in which the output sample can be represented without losing a significant bit, and

(2) the largest dynamic range selected for a previously processed output sample in the stage.

22. The device of claim 18, further comprising a pre-calculation module coupled to the calculation module, the pre-calculation module adapted to normalize the dynamic ranges of the input samples.

23. The device of claim 18, further comprising a final stage processor coupled to the post-calculation module, the final stage processor adapted to normalize the dynamic ranges of the output samples of a final stage.

24. The processor of claim 23, further comprising a dynamic range summer coupled to the post-calculation module, the dynamic range summer adapted to calculate a cumulative decrease in dynamic range over the multiple stages.

25. The processor of claim 23, wherein the final stage processor is adapted to increase the dynamic ranges of the output samples of the final stage by a cumulative decrease in dynamic range over the multiple stages.

26. A multi-stage digital signal processor comprising:

a calculation module adapted to compute a first set of output samples using a first set of input samples;

a post-calculation module operatively coupled to the calculation module, the post-calculation module adapted to decrease the dynamic range of at least one of the first set of output samples if the first set output sample can be represented in a smaller dynamic range without losing a significant bit; and

a second calculation module coupled to the post-calculation module, the second calculation module adapted to compute a second set of output samples using a second set of input samples, the second set of input samples corresponding to the first set of output samples.

27. A device for processing a digital signal in multiple stages, the device comprising:

a plurality of stage modules operatively coupled together, the stage modules adapted to process one or more stages, a stage module comprising:

a calculation module adapted to compute a set of output samples using a set of input samples; and

a post-calculation module operatively coupled to the calculation module, the post-calculation module adapted to decrease the dynamic range of at least one of the output samples if the output sample can be represented in a smaller dynamic range without losing a significant bit;

wherein the set of output samples for a particular stage module is used for the set of input samples for a next stage module.

28. The processor of claim 27, wherein at least two stage modules share a calculation module.

29. A device for processing a digital signal in a series of consecutive stages in which a set of output samples for one stage corresponds to a set of input samples for a subsequent stage, the device comprising:

a storage means for storing the input and output samples of each stage;

a calculation means, for each stage, for computing a set of output samples using a set of input samples; and

a postprocessing means for increasing the number of least significant bits retained for an output sample without losing a significant bit.

30. The device of claim 29, wherein the postprocessing means comprises a means for adjusting the dynamic range of an output sample.

31. A DSL modem comprising:

an input port for receiving a data signal;

a digital signal processor adapted to receive the data signal from the input port and process the data signal in multiple stages, each stage resulting in a plurality of output samples derived from a plurality of input samples, wherein the digital signal processor is adapted to decrease the dynamic range of one or more output samples of one or more stages without losing a significant bit; and

an interface coupled to the digital signal processor for receiving therefrom a processed data signal, the processed data signal corresponding to a plurality of output samples from one of the stages.

32. The modem of claim 31, further comprising:

an analog front-end coupled to the interface, the analog front end adapted to convert the data signal to an analog format for being transmitted over a local loop.

33. The modem of claim 31, wherein the digital signal processor performs discrete multi-tone modulation on the data signal in one or more of the stages.